REMARKS

Claims 1-8 are now pending in the application. The Examiner is respectfully requested to reconsider and withdraw the rejections in view of the amendments and remarks contained herein.

REJECTION UNDER 35 U.S.C. § 102

Claims 1, 3, 5 and 7 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Iwata et al. (U.S. Pat. No. 5,999,022). This rejection is respectfully traversed.

The Examiner alleges that Iwata discloses a second circuit 3 generating a clock signal detection result. Applicant respectfully submits that Iwata does not disclose a second circuit that generates a clock signal detection result in accordance with Applicant's invention. Applicant's invention is directed to a clock signal detection circuit that indicates whether a device is receiving a clock signal. A second circuit generates a clock signal detection result that indicates whether the device is receiving the clock signal.

Applicant amends claim 1 to clarify that the impedance element "maintains the output signal above a first threshold when the output terminal is in the high impedance state for less than a first period." Further, the clock signal detection result "is a first state when the output signal is above the first threshold and is a second state when the output signal is below the first threshold, wherein the output signal decreases below the first threshold when the output terminal is in the high impedance state for greater than or equal to the first period." Iwata does not show, teach, or suggest such a structure.

Referring to FIG. 4B of Iwata, an output signal (at output terminal D0) of the first circuit 2 is Vref when the clock signal is high and the output terminal is in a high impedance state. When the clock signal is low, the output signal is Vh or Vl according to an input signal IN. When the output terminal is in the high impedance state, the output signal is Vref. An impedance element does not maintain the output signal above a first threshold when the output terminal is in the high impedance state for less than a first period. The output signal does not decrease below a threshold after a first period. In other words, the output signal is a constant value Vref for as long as the output terminal is in the high impedance state. Therefore, the second circuit 3 does not generate a clock signal detection result that is a first state when the output signal is above the first threshold and is a second state when the output signal is below the first threshold according to the influence of the impedance element as described above.

Applicant respectfully submits that claim 1, as well as its corresponding dependent claim, should be in condition for allowance. Applicant amends claim 5 to include subject matter analogous to claim 1. Therefore, claim 5, as well as its corresponding depending claims, should be allowable for the same reasons.

ALLOWABLE SUBJECT MATTER

The Examiner states that claims 2, 4, 6, and 8 are allowed. Applicant thanks the Examiner for the allowed claims.

CONCLUSION

It is believed that all of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider and withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Office Action, and as such, the present application is in condition for allowance. Thus, prompt and favorable consideration of this amendment is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (248) 641-1600.

Respectfully submitted,

Dated: Aug 18, 2005

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